SDLS075

- Parallel Inputs and Outputs
- Four Operating Modes: Synchronous Parallel Load Right Shift Left Shift Do Nothing
- Positive Edge-Triggered Clocking
- Direct Overriding Clear

түре	TYPICAL MAXIMUM CLOCK FREQUENCY	TYPICAL POWER DISSIPATION
'19 4	36 MHz	195 mW
'LS194A	36 MHz	75 mW
' S194	105 MHz	425 mW

description

These bidirectional shift registers are designed to incorporate virtually all of the features a system designer may want in a shift register. The circuit contains 46 equivalent gates and features parallel inputs, parallel outputs, right-shift and left-shift serial inputs, operating-mode-control inputs, and a direct overriding clear line. The register has four distinct modes of operation, namely:

Inhibit clock (do nothing) Shift right (in the direction Q_A toward Q_D) Shift left (in the direction Q_D toward Q_A) Parallel (broadside) load

Synchronous parallel loading is accomplished by applying the four bits of data and taking both mode control inputs, SO and S1, high. The data are loaded into the associated flip-flops and appear at the outputs after the positive transition of the clock input. During loading, serial data flow is inhibited.

Shift right is accomplished synchronously with the rising edge of the clock pulse when SO is high and S1 is low. Serial data for this mode is entered at the shift-right data input. When SO is low and S1 is high, data shifts left synchronously and new data is entered at the shift-left serial input.

Clocking of the shift register is inhibited when both mode control inputs are low. The mode controls of the SN54194/SN74194 should be changed only while the clock input is high.

SN54194, SN54LS194A, SN54S194, SN74194, SN74LS194A, SN74S194 4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTERS March 1974-REVISED MARCH 1988

MARCH 1974-REVISED MARCH 1988



SN54LS194A, SN54S194 . . . FK PACKAGE (TOP VIEW)



NC - No internal connection

logic symbol[†]



[†]This symbol is in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.

Pin numbers shown are for D. J. N. and W packages.

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SN54194, SN54LS194A, SN54S194 SN74194, SN74LS194A, SN74S194 **4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTERS**

					FUNCTIO	N T	ABLE			<u> </u>	OUT	PUTS		1
	мо	DE			RIAL		PARA		L		· · · · ·	_		1
CLEAR	S1	SO	CLOCK	LEFT	RIGHT	A	в	С	D	QA	QB	QC	αD	
L	x	X	х	X	x	X	х	х	Х	L	L	L	٢	
H	х	х	L	x	x	X	х	х	х	Q _{A0}	QB0	Q_{CO}	apo	
н	н	н	1	x	х	а	b	с	d	а	b	с	đ	
н	L	н	Ť	х	H.	X	х	x	×	н	Q _{An}	QBn	Q _{Cn}	
н	L	н	†	х	L	x	х	х	х	L	0 _{An}	0 _{Bn}	Q _{Сп}	
н	н	L.	Ť	н	х	x	x	х	х	QBn	Q _{Cn}	a _{Dn}	н	
н	н	L	1 T	L	х	х	х	х	х	QBn	QCn	Q _{Dn}	Ŀ	ľ
н	L	ւ	×	x	x	х	х	х	х	O _{AO}	OB0	Q _{C0}	QDO	1

- high level (steady state)
 - low level (steady state)
- irrelevant (any input, including transitions)
- transition from low to high level
- c, d = the level of steady-state input at inputs A, B, C, or D, respectively.
- $(0, \Omega_{BO}, \Omega_{CO}, \Omega_{DO})$ the level of Ω_A , $\Omega_B, \Omega_C, \text{ or } \Omega_D$, respectively, before the indicated steady-state input conditions were established.
- $n, Q_{Bn}, Q_{Cn}, Q_{Dn} =$ the level of Q_A , QB, QC, respectively, before the mostrecent T transition of the clock.

schematics of inputs and outputs







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SN54LS194A, SN54S194 SN74LS194A, SN74S194 4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTERS



TEXAS INSTRUMENTS

SN54194, SN54LS194A, SN54S194, SN74194, SN74LS194A, SN74S194 4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTERS



typical clear, load, right-shift, left-shift, inhibit, and clear sequences



SN54194, SN74194 **4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTERS**

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V _{CC} (see Note 1)		,			•												7 V
Input voltage																	
Operating free-air temperature range: SN54194	•			1	•									_	55°	C to	125°C
SN74194															0	°Cı	o 70°C
Storage temperature range	•						•	•	•	•	•	•		_	65°	C to	150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

			SN5479	4		SN7419	4	UNIT
		MIN	NÔM	MAX	MIN	NOM	MAX	UNIT
Supply voltage, V _{CC}		4.5	5	5,5	4.75	5	5.25	V
High-level output current, IOH				-800			-800	μA
Low-level output current, IOL				16			16	mA
Clock frequency, fclock		0		25	0		25	MHz
Width of clock or clear pulse, tw		20			20			ns
	Mode control	30			30			ns
Setup time, t _{su}	Serial and parallel data	20			20			ns
	Clear inactive-state	25			25			ns
Hold time at any input, t _h		0			0			ns
Operating free-air temperature, TA		-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

-			Nortoust		SN5419	4		SN7419	4	
	PARAMETER	TESTCO	NDITIONS	MIN	түр‡	мах	MIN	TYP‡	MAX	UNIT
∀ін	High-level input voltage			2			2			V
VIL	Low-level input voltage					0.8			0.8	V
VIK	Input clamp voltage	V _{CC} = MIN,	lj =12 mA			-1.5			-1.5	V
vон	High-level output voltage	V _{CC} = MIN, V _{IL} = 0.8 V,	V _{IH} = 2 V, I _{OH} = -800 μA	2.4	3.4		2.4	3.4		v
Vol	Low-level output voltage	V _{CC} = MIN, VIL = 0.8 V,	V _{IH} = 2 V, IOL = 16 mA		0.2	0.4		0.2	0.4	v
<u>η</u>	Input current at maximum input voltage	V _{CC} = MAX,	V1 = 5.5 V			1			1	mA
пн	High-level input current	V _{CC} = MAX,	V _I = 2.4 V			40			40	μA
41	Low-level input current	VCC = MAX,	Vi = 0.4 V			-1.6	_		-1.6	mA
los	Short-circuit output current §	V _{CC} = MAX		-20		-57	-18		-57	mA
lcc	Supply current	V _{CC} = MAX,	See Note 2		39	63		39	63	mA

[†]For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[‡]All typical values are at $V_{CC} = 5 V$, $T_A = 25^{\circ}C$. §Not more than one output should be shorted at a time.

NOTE 2: With all outputs open, inputs A through D grounded, and 4.5 V applied to S0, S1, clear, and the serial inputs, I_{CC} is tested with a momentary GND, then 4.5 V applied to clock.

switching characteristics, VCC = 5 V, TA = 25 °C

	PARAMETER	TEST CONDITIONS	MIN	ТҮР	MAX	UNIT
fmax	Maximum clock frequency	- C(= 15 pF,	25	36		MHz
TPHL	Propagation delay time, high-to-low-level output from clear	$- R_{I} = 400 \Omega_{r}$		19	30	ns
tPLH	Propagation delay time, low-to-high-level output from clock	- See Figure 1		14	22	ns
tPHL	Propagation delay time, high-to-low-level output from clock	Jee rigure i		17	26	ns

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SN54LS194A, SN74LS194A 4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTERS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC (see Note 1) .											•			7 V
Input voltage														7 V
Operating free-air temperature range:														
	SN74LS194A	-		. ,								0°C	to 7	0°C
Storage temperature range			•				-		٠	•	-65	δ°C t	o 15	О°С
 a tatan ing tahun sina si														

NOTE 1: Voltage values are with respect to network ground terminal,

recommended operating conditions

		SN	54LS19	4A	SN	74LS19	94A	
		MIN	NOM	MAX	MIN	NOM	MAX	UNIT
Supply voltage, VCC		4.5	5	5.5	4.75	5	5.25	V
High-level output current, IOH	_			-400			-400	μA
Low-level output current, IOL	······································	1		4	1		8	mA
Clock frequency, fclock		0		25	0		25	MHz
Width of clock or clear pulse, tw		20			20			ns
	Mode control	30			30			D 5
Setup time, t _{su}	Serial and parallel data	20			20			ns
	Clear inactive-state	25			25			ns
Hold time at any input, ^t h		0			0			ns
Operating free-air temperature, TA		-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	PARAMETER				SN	54LS19	4A	SN	74LS19	4A	
	PARAMETER		SICUNDIIN	JNS'	MIN	TYP‡	MAX	MIN	TYP‡	MAX	UNIT
VIH	High-level input voltage				2			2			V
VIL	Low-level input voltage						0.7			0.8	V
٧ı	Input clamp voltage	V _{CC} = MIN,	lı ≈ −18 mA	4	1		-1.5			-1.5	• V
۷он	High-level output voltage	V _{CC} = MIN, V _{IL} = V _{IL} max	V _{IH} = 2 V, , I _{OH} = -400	μA	2.5	3.5		2.7	3,5		v
¥		V _{CC} = MIN,	V _{IH} = 2 V,	IOL = 4 mA		0.25	0.4	<u> </u>	0.25	0.4	v
VOL	Low-level output voltage	VIL = VIL max		1 _{0L} = 8 mA					0.35	0.5	v
4	Input current at maximum input voltage	V _{CC} = MAX,	V ₁ = 7 V				0.1			0.1	mA
Чн	High-level input current	V _{CC} = MAX,	VI = 2.7 V				20			20	μA
μL	Low-level input current	V _{CC} = MAX,	V ₁ = 0.4 V				-0,4			-0.4	mΑ
los	Short-circuit output current §	V _{CC} = MAX			-20		-100	-20		-100	mА
Icc	Supply current	V _{CC} = MAX,	See Note 2		1	15	23		15	23	mА

[†]For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

NOTE 2: With all outputs open, inputs A through D grounded, and 4.5 V applied to S0, S1, clear, and the serial inputs, I_{CC} is tested with a momentary GND, then 4.5 V, applied to clock.

switching characteristics, $V_{CC} = 5 V$, $T_A = 25 °C$

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
fmax	Maximum clock frequency	Ci = 15 pF	25	36		MHz
^t PHL	Propagation delay time, high-to-low-level output from clear	CL = 15 pF, Βι = 2 kΩ,		19	30	ns
^t PLH	Propagation delay time, low-to-high level output from clock	See Figure 1		14	22	វាន
tPHL	Propagation delay time, high-to-low level output from clock	See Figure 1		17	26	ns

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SN54S194, SN74S194 4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTERS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V _{CC} (see Note 1)			-															•	7V
Input voltage		•			•														5.5V
Operating free-air temperature range:	SN54S194		-	-	-	-							-	-					–55°C to 125°C
	SN74S194											•				•			. 0°C to 70°C
Storage temperature range		•	٠	•	•	• •	•••	•	• •	•	•	•	•	•	•	•	·	-	–65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		5	SN5451	94	5	SN74S19	94	l
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V _{CC}	<u>_</u>	4.5	5	5.5	4.75	5	5.25	V
High-level output current, IOH		1		-1	· · · ·		1	mA
Low-level output current, IOL		1		20	—		20	mA
Clock frequency, fclock		0		70	0		70	MHz
Width of clock pulse, tw(clock)		7			7	•		ns
Width of clear pulse, tw(clear)		12			12			ns
	Mode control	11	_		11			ns
Setup time, t _{su}	Serial and parallel data	5			5			пѕ
	Clear inactive-state	9			9			ns
Hold time at any input, t _h	····	3			3			ns
Operating free-air temperature, TA		-55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

[PARAMETER	TEST CONDITIONS [†]	SN54S194			SN74S194			
i		TEST CONDITIONS	MIN	TYP [‡]	MAX	MIN	TYP [‡]	MAX	TINU
Ин	High-level input voltage		2			2			v
VIL	Low-level input voltage		1		0.8		·	0.8	V
Viк	Input clamp voltage	V _{CC} = MIN, I ₁ =18 mA	1		-1.2			-1.2	V
∨он	High-level output voltage	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = 0.8 V, V _{OH} = -1 mA	2,5	3.4		2.7	3.4		V
Vol	Low-level output voltage	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = 0.8 V, I _{OL} = 20 mA			0.5			0.5	v
1	Input current at maximum input voltage	V _{CC} = MAX, V ₁ = 5.5 V	1		1			1	mA
ίн	High-level input current	V _{CC} = MAX, V ₁ = 2.7 V	<u> </u>		50			50	μA
1L	Low-level input current	V _{CC} = MAX, V _I = 0.5 V		-	-2	-		2	mA
los	Short-circuit output current§	V _{CC} = MAX	-40		-100	-40		-100	mA
	Supply current	VCC = MAX, See Note 2	1	85	135		85	135	-
lcc		V _{CC} = MAX, T _A = 125°C, W package See Note 2			110				mA

[†]For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[‡]All typical values are at $V_{CC} = 5 V$, $T_A = 25^{\circ}C$.

 ${
m \$}$ Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

NOTE 2: With all outputs open, inputs A through D grounded, and 4.5 V applies to S0, S1, clear, and the serial inputs, I_{CC} is tested with a momentary GND, then 4.5 V, applied to clock.

switching characteristics, V_{CC} = 5 V, T_A = 25 °C

[PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
fmax	Maximum clock frequency	0	70	106		MHz
TPHL	Propagation delay time, high-to-low-level output from clear	− C _L ≈ 15 pF,		12.5	18.5	ns
^t PLH	$R_{L} = 280 \ \Omega,$ $R_{L} = 280 \ \Omega,$		4	8	12	nŝ
t PHL	Propagation delay time, high-to-low-level output from clock	See Figure 1	4	11	16.5	nS



SN54194, SN54LS194A, SN54S194, SN74194, SN74LS194A, SN74S194 4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTERS

PARAMETER MEASUREMENT INFORMATION



LOAD FOR OUTPUT UNDER TEST

. TEST TABLE FOR SYNCHRONOUS INPUTS

DATA INPUT			OUTPUT TESTED (SEE NOTE E)			
FOR TEST	S1	S 0				
A	4.5 V	4.5 V	Ω _A at t _{n+1}			
В	4.5 V	4.5 V	QB at tn+1			
с	4.5 V	4.5 V	QC at tn+1			
D	4.5 V	4.5 V	QD at tn+1			
L Serial Input	4.5 ∨	0 V	Q _A at t _{n+4}			
R Serial Input	٥v	4.5 V	QD at tn+4			



NOTES: A. The clock pulse generator has the following characteristics: $Z_{out} \approx 50 \Omega$ and PRR \leq 1 MHz, For '194, $t_r \leq$ 7 ns and $t_f \leq$ 7 ns. For 'LS194A, $t_r \leq$ 15 ns and $t_f \leq$ 6 ns. For 'S194, $t_r \leq$ 2.5 ns and $t_f \leq$ 2.5 ns. When testing f_{max}, vary PRR.

- B. C₁ includes probe and jig capacitance.
- C. All diodes are 1N3064 or 1N916.
- D. A clear pulse is applied prior to each test.
- E. For '194 and 'S194, V_{ref} = 1.5 V; for 'LS194A, V_{ref} = 1.3 V.
- F. Propagation delay times (tpLH and tpHL) are measured at tn+1. Proper shifting of data is verified at tn+4 with a functional test.
- G. $t_n = bit time before clocking transition.$
 - t_{n+1} = bit time after one clocking transition. t_{n+4} = bit time after four clocking transitions.

FIGURE 1-SWITCHING TIMES



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